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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,851	JADON ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *2-3, 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/824,851 filed on 4/14/2004.

2. Claims 1-15 have been submitted and examined.

Claim Objections

3. Claims 2-3 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to directly or indirectly refer to an independent claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 2 is written as being dependent on claim 3, while claim 3 is written to be dependent on claim 2. Either claim in this loop does not depend upon an independent claim.

4. Claim 5 is objected to because of the following informalities:

   a. Claim 5 states the term "optionally..." this does not realize the limitations following the term. For example, a microprocessor can optionally navigate the way to the moon, but that does not mean it is actually doing it. Optionally doing something is no different from not specifying whether it is done or not. The inclusion or exclusion of those limitations does not change the scope of the claim.

   Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-15 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Regarding claim 1, the phrase "having the ability" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d). It is unclear if the host computer actually directly controls the NVRAM device. Having the ability to do something does not provide a resolution to it being done or not. For example, a person has the ability to jump off of a building, but that has no bearing on whether or not they actually do.

8. With respect to claim 2, it depends on a claim (claim 3) that depends on claim 2, which creates confusion, indefiniteness, and lacks clear metes and bounds.

9. With respect to claim 3, it depends on a claim (claim 2) that depends on claim 3, which creates confusion, indefiniteness, and lacks clear metes and bounds. Additionally, claim 3 is confusing and indefinite as it appears to be claiming the host computer. The independent claim (claim 1) merely states that the controller "can be connected to a host computer" and does not claim the combination of the controller and a host computer. This adds additional confusion to the claim.

10. With respect to claim 5, the claim is confusing and indefinite as it appears to be claiming a method of the host computer. The parent claim (claim 1) merely states that

the controller "can be connected to a host computer" and does not claim the combination of the controller and a host computer.

11. With respect to claims 4-6, 8, and 10-12, the claims are confusing and indefinite as each claim refers to either "the disk controller(s)" or "the disk array controllers". The parent claim (independent claim 1) recites a "host-NVRAM disk-array controller" and a "plurality of disk array controllers". It is unclear in claims 4-6, 8, and 10-12 which disk controller the applicant is talking about.

If in the case of claim 6, the applicant is talking about the plurality of disk array controllers, claim 6 would be rejected under the fourth paragraph of 35 U.S.C. 112 because it is impossible to have ***a plurality*** of disk controllers and ***only one*** disk controller at the same time.

12. The claims not specifically mentioned are rejected because of their dependency.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. Claims 1, 5-7, 10, 12, 14-15 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader at al., US patent application publication 2001/0001871 and Kikuchi et al., US patent 6,131,139.

17. With respect to claim 1, Shrader teaches of a host-NVRAM disk-array controller that can be connected to a host computer, the controller comprising: an NVRAM connected to a memory controller (together called the NVRAM device) (fig. 3; items 62, 82; paragraph 0027),

a plurality of disk array controllers (fig. 3; items 54a, 54b);

a plurality of buses connecting the NVRAM device and the disk array controllers (fig. 3; item 84, 96, 98; paragraph 0029-0030).

Kikuchi teaches of the host computer having the ability to directly control the NVRAM device (column 1, lines 25-29; flash memory is a type of non-volatile RAM);

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader and Kikuchi at the time of the invention to have the host computer directly control the NVRAM in Shrader as taught in Kikuchi. Their motivation would have been to increase speed of data transfer between the host computer and the NVRAM device by giving the host computer a direct pipeline to access the NVRAM device.

18. With respect to claim 5, Shrader teaches of the method comprising of the host computer performing steps: allocating memory from NVRAM or recognizing during booting that the memory was previously allocated (paragraph 0022-0023; where the NVRAM contains a memory map of storage space in the disk array, a read cache and a write cache. It is abundantly clear to one of ordinary skill in the art that by having space for read and write caches, that memory has been allocated for such caches);

freeing memory from NVRAM with or without first writing to the disk array controllers (paragraph 0023; as each read and write cache stores the data before it is transferred into or out of the disk array, there must be a way to free the memory in each respective cache when it fills, else it would no longer be able to store data in the memory)

optionally writing or updating data in NVRAM from host memory (paragraph 0023; as the write cache stores data written to the disk array, it is abundantly clear that it is being written by the host computer, and thus from a memory in the host computer);

optionally reading data from NVRAM to host memory (paragraph 0023; as the read cache stores data read out from the disk array, it is abundantly clear that it is being read by the host computer, and thus stored in a memory in the host computer);

optionally scheduling data transfers from NVRAM to the disk array controllers (paragraph 0021, 0029);

optionally scheduling data transfers from the disk array controllers to NVRAM (paragraph 0021, 0029);

19. With respect to claim 6 Shrader teaches of wherein there is only one disk controller (fig. 1; paragraph 0020-0021; where the data storage system has one disk array controller which has two identical boards. Additionally, it is abundantly clear to one of ordinary skill in the art that the identical controller boards can be replaced with a single board eliminating the redundant functionality in order to reduce the overhead, lower the cost, and reduce the physical size of the system).

20. With respect to claim 7, Shrader teaches of wherein the memory controller is on a separate bus from the disk controllers to allow it to operate at a different speed and using a different bus protocol (fig. 3; paragraph 0028-0030; where the memory transaction manager is on a PCI bus, 86 and the disk controllers are on an 1^2C, 98 and point-to-point bus, 96. As these busses are different protocols, they are operating at different speeds).

21. With respect to claim 10, Shrader teaches of wherein the disk controllers are SCSI controllers (paragraph 0020; where the controller is coupled to the disk array through a SCSI connection, thus the controller must support it. Additionally, the applicant admits such as prior art in paragraph 0007 of the specification).

22. With respect to claim 12, Shrader teaches of wherein the disk controllers are Fibre Channel controllers (paragraph 0026; where the I/O modules of the disk controller

employ fibre channel technology, thus they must support such. Additionally, the applicant admits such as prior art in paragraph 0007 of the specification).

23. With respect to claim 14, Shrader teaches of wherein the NVRAM can operate from external power (paragraph 0026; where the power supply provides power to the components in the controllers).

24. With respect to claim 15, Shrader teaches of wherein the NVRAM can preserve data without any power (paragraph 0021; where the mirrored memory is battery backed NVRAM; as the definition of NVRAM is a RAM that holds its data when power is removed).

25. Claim 2-3 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 1 above, and further in view of Endsley US patent 6438683.

26. With respect to claim 2, Endsley teaches of wherein the memory controller can act as a DMA master (fig. 3; column 5, lines 56-64).

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Endsley at the time of the invention to have the memory manager of the combination of Shrader and Kikuchi act as a DMA controller as taught in Endsley. Their motivation would have been to provide DMA data transfer to and from the NVRAM thus, eliminating the need for the processor to control the transfer, which allows the processor to spend its processing time elsewhere, making this rune more efficiently (Endsley, column 1, lines 17-25).

27. With respect to claim 3, Endsley teaches of the method comprising of the host computer programming the memory controller as a DMA master for transferring data between host memory and the memory (fig. 3; column 5, lines 56-64; in the combination of Shrader, Kikuchi and Endsley, the DMA transfer would be between the NVRAM and the host computer's memory).

28. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 1 above, and further in view of Endsley US patent 6438683.

29. With respect to claim 4, Nelson teaches of the method comprising of transferring data directly between the memory and the disk array controllers using DMA on the memory controller or on the disk array controllers (fig. 1; column 3, lines 12-16; in the combination of Shrader, Kikuchi and Nelson, the memory would be the NVRAM of Shrader).

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Nelson at the time of the invention to use DMA transfer to mirror the NVRAM in the combination of Shrader and Kikuchi as taught in Nelson. Their motivation would have been to have realtime mirrored memory (Nelson column 3, lines 12-16).

30. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 7 above, and further in view of Buckland et al. US patent 6581129.

31. With respect to claim 8, Shrader teaches of wherein the NVRAM controller is on a PCI 2.2 bus (fig. 3; paragraph 0028; where bus 86 is a PCI bus. it is abundantly clear

to one of ordinary skill in the art that the PCI bus can be implemented with the PCI v2.2 protocol as it is a current conventional PCI version).

Buckland teaches of the disk controllers on a faster PCI-X bus (column 1, lines 15-36).

32. It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Buckland at the time of the invention to use a PCI-X bus connecting the disk controllers in the combination of Shrader and Kikuchi as taught in Buckland. Their motivation would have been to improve performance between controllers (Buckland column 1, lines 34-37).

33. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 1 above, and further in view of Munguia et al., US patent application publication 2004/0236923.

34. With respect to claim 9, Munguia teaches of buses that are Conventional PCI, PCI-X, and PCI Express buses (fig. 3; paragraph 0029; furthermore as stated in the claim, the applicant admits that the use of PCI, PCI-X, and PCI Express busses is conventional).

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Munguia at the time of the invention to use PCI, PCI-X, and PCI Express busses for the busses of the combination of Shrader and Kikuchi as taught in Munguia. Their motivation would have been to provide various a modern, high performance, low latency bus protocol (Munguia, paragraph 0003).

35. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 1 above, and further in view of Ooi, US patent 6961787.

36. With respect to claim 11, Shrader fails to explicitly teach of wherein the disk controllers are SATA controllers.

However, Ooi, teaches of wherein the disk controllers are SATA controllers (fig. 1, 2; item 20; column 2, lines 8-10).

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Ooi at the time of the invention to make the controllers of the combination of Shrader and Kikuchi SATA controllers and the disks SATA disks as taught in Ooi. Their motivation would have been to provide forward and backwards compatibility, scalability and evolutionary enhancement to the system in addition to higher transfer speeds at a lower cost (Ooi, column 1, lines 21-30).

37. Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 1 above, and further in view of Mason, JR. et al., US patent application publication 2003/0135674.

38. With respect to claim 13, Shrader teaches of a battery backup powered NVRAM (paragraph 0021), but doesn't explicitly teach of an SDRAM being the battery-backed NVRAM.

Mason teaches of a battery-backed SDRAM (fig. 2; paragraph 0050).

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Mason at the time of the invention to use the battery backed SDRAM of Mason as the NVRAM in the combination of Shrader and Kikuchi. Their

motivation would have been to provide the high speed accessing of SDRAM as a non-volatile memory (Mason paragraph 0002).

39. Additionally, claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi with the following interpretation.

40. With respect to claim 1, Shrader teaches of a host-NVRAM disk-array controller that can be connected to a host computer, the controller comprising: an NVRAM connected to a memory controller (together called the NVRAM device) (fig. 1-3; items 62, 40; paragraph 0020-0023; as the RAID management system runs on the processor, 40, the processor controls what is stored to the disk array through the NVRAM and where it is stored based on the memory map in the NVRAM),

a plurality of disk array controllers (fig. 3; items 54a, 54b);

a plurality of buses connecting the NVRAM device and the disk array controllers (fig. 1-3; items 26, 84, 96, 98; and the bus shown in figure 2 connecting the components on the computer).

Kikuchi teaches of the host computer having the ability to directly control the NVRAM device (column 1, lines 25-29; flash memory is a type of non-volatile RAM);

It would have been obvious to one of ordinary skill in the art having the teachings of Shrader and Kikuchi at the time of the invention to have the host computer directly control the NVRAM in Shrader as taught in Kikuchi. Their motivation would have been to increase speed of data transfer between the host computer and the NVRAM device by giving the host computer a direct pipeline to access the NVRAM device

41. With respect to claim 7, Shrader teaches of wherein the memory controller is on a separate bus from the disk controllers to allow it to operate at a different speed and using a different bus protocol (fig. 1-3; paragraph 0027-0030; where the processor 40 is on the bus shown in fig 2, connecting through the I/O module, converter, bus 80, memory transaction manager, and bus 84 to NVRAM. The disk controllers are connected through busses 96 and 98. As these busses are different protocols, they are operating at different speeds).

42. Claim 8 is additionally rejected under 35 U.S.C. 103(a) as being unpatentable over Shrader and Kikuchi as applied to claim 7, and further in view of Buckland et al. US patent 6581129.

43. With respect to claim 8, Shrader teaches of wherein the NVRAM controller is on a PCI 2.2 bus (fig. 3; paragraph 0028; where the processor 40 is connected to the NVRAM through the computer bus, I/O module, and busses 80, 84. Bus 80 is a PCI bus. It is abundantly clear to one of ordinary skill in the art that the PCI bus can be implemented with the PCI v2.2 protocol as it is a current PCI version).

Buckland teaches of the disk controllers on a faster PCI-X bus (column 1, lines 15-36).

44. It would have been obvious to one of ordinary skill in the art having the teachings of Shrader, Kikuchi and Buckland at the time of the invention to use a PCI-X bus connecting the disk controllers in the combination of Shrader and Kikuchi as taught in Buckland. Their motivation would have been to improve performance between controllers (Buckland column 1, lines 34-37).

45. Claims 1-15 are also rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's admitted prior art (AAPA) and Kikuchi.

46. With respect to claims 1-15, the Applicant's admitted prior art teaches of all the claimed limitations except for the host computer having the ability to directly control the NVRAM device (paragraph 0033 of the specification. The applicants states, "The methods above are not by themselves new," thus the methods and all they entail are admitted prior art).

Kikuchi teaches of host computer having the ability to directly control the NVRAM device (column 1, lines 25-29; flash memory is a type of non-volatile RAM).

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Kikuchi at the time of the invention to have the host computer directly control the NVRAM in AAPA as taught in Kikuchi. Their motivation would have been to increase speed of data transfer between the host computer and the NVRAM device by giving the host computer a direct pipeline to access the NVRAM device.

47. Claims 1-15 are also rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's admitted prior art (AAPA) and Scharland, et al., WO 97/24655.

48. With respect to claims 1-15, the Applicant's admitted prior art teaches of all the claimed limitations except for the host computer having the ability to directly control the NVRAM device (paragraph 0033 of the specification. The applicants states, "The methods above are not by themselves new," thus the methods and all they entail are admitted prior art).

Scharland teaches of a host computer having the ability to directly control the memory device (abstract).

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Scharland at the time of the invention to have the host computer directly control the NVRAM in AAPA as taught in Scharland. Their motivation would have been to greatly reduce the cost (Scharland, abstract).

Conclusion

49. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

50. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

51. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

52. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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